IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR L.L.C., Plaintiffs, v. ON SEMICONDUCTOR CORP. and SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC, Defendants.	Civil Action No. 06-720 (JJF)
ON SEMICONDUCTOR CORP. and SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC, Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR L.L.C., Defendants.	Civil Action No. 07-449 (JJF)

DECLARATION OF JASON CHOY IN SUPPORT OF SAMSUNG'S ANSWERING BRIEF IN SUPPORT OF ITS PROPOSED CLAIM CONSTRUCTIONS

I, Jason Choy, declare as follows:

1. I am admitted to this Court *pro hac vice* and am an associate with the law firm of Kirkland & Ellis LLP, counsel of record for Samsung Electronics Co., Ltd., *et al.*, as plaintiffs in Civil Action No. 06-720 (JJF) and defendants in Civil Action No. 07-449 (JJF).

2. Attached hereto as Exhibit CC is a true and correct copy of U.S. Patent No. 4,855,251.

3. Attached hereto as Exhibit DD is a true and correct copy of U.S. Patent No. 4,263,606.

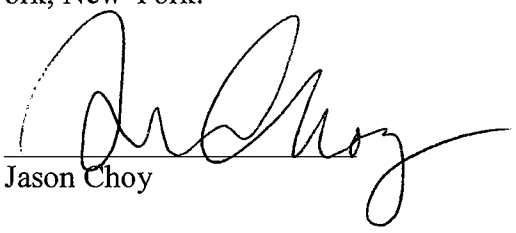
4. Attached hereto as Exhibit EE is a true and correct copy of excerpts from MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS (4th ed. 1989).

5. Attached hereto as Exhibit FF is a true and correct copy of a letter dated April 27, 2008 from Guadalupe M. Garcia to John C. Spaccarotella.

6. Attached hereto as Exhibit GG is a true and correct copy of U.S. Patent No. 4,870,472.

7. Attached hereto as Exhibit HH is a true and correct copy of excerpts from MCGRAW-HILL ELECTRONICS DICTIONARY (5th ed. 1994).

I declare under penalty of perjury of the laws of the United States that the foregoing is true and correct. Executed April 28, 2008, in New York, New York.



Jason Choy

CERTIFICATE OF SERVICE

I, Andrew A. Lundgren, Esquire, hereby certify that on April 28, 2008, I caused to be electronically filed a true and correct copy of the foregoing document with the Clerk of the Court using CM/ECF, which will send notification that such filing is available for viewing and downloading to the following counsel of record:

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I further certify that on April 28, 2008, I caused a copy of the foregoing document to be served by hand delivery and e-mail on the above-listed counsel of record and on the following non-registered participants in the manner indicated:

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EXHIBIT CC

United States Patent [19]

Iyogi et al.

[11] **Patent Number: 4,855,251**

[45] **Date of Patent: Aug. 8, 1989**

[54] **METHOD OF MANUFACTURING ELECTRONIC PARTS INCLUDING TRANSFER OF BUMPS OF LARGER PARTICLE SIZES**

[75] Inventors: **Kiyoshi Iyogi; Koji Yamakawa,** both of Tokyo; **Nobuo Iwase,** Kamakura, all of Japan

[73] Assignee: **Kabushiki Kaisha Toshiba,** Kawasaki, Japan

[21] Appl. No.: **267,707**

[22] Filed: **Nov. 3, 1988**

Related U.S. Application Data

[63] Continuation of Ser. No. 64,397, Jun. 22, 1987, abandoned.

[30] **Foreign Application Priority Data**

Jun. 26, 1986 [JP] Japan 61-150445

[51] **Int. Cl.**[4] **H01L 21/92**

[52] **U.S. Cl.** **437/183;** 437/182; 437/230; 437/172

[58] **Field of Search** 437/183, 187, 203, 245, 437/182, 170, 172, 230; 357/67, 71; 204/47.5, 52.1, 52.5

[56] **References Cited**

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Hatada et al., "New Film Carrier Assembly Technology Transferred Bump Tab", Proc. IEEE 1986 Symposium, Sep. 1986, pp. 122–127.

Primary Examiner—Brian E. Hearn
Assistant Examiner—T. N. Quach
Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt

[57] **ABSTRACT**

According to the present invention, a method is provided of manufacturing electronic parts, comprising a first step of forming on the surface of a substrate a bump wherein the metal particles of that portion of the bump which contacts the surface of the substrate have a larger diameter than the metal particles of that portion of the bump which does not contact the surface of the substrate, a second step of transferring the bump to an electrode lead, and a third step of connecting an electrode lead to a predetermined electrode section of the semiconductor chip, by means of the transferred bump. The method of the present invention ensures that the bump does not fall off during the electroplating and washing steps, and ensures a high-strength bond between the transferred bump and the electrode section of a semiconductor chip.

9 Claims, 2 Drawing Sheets

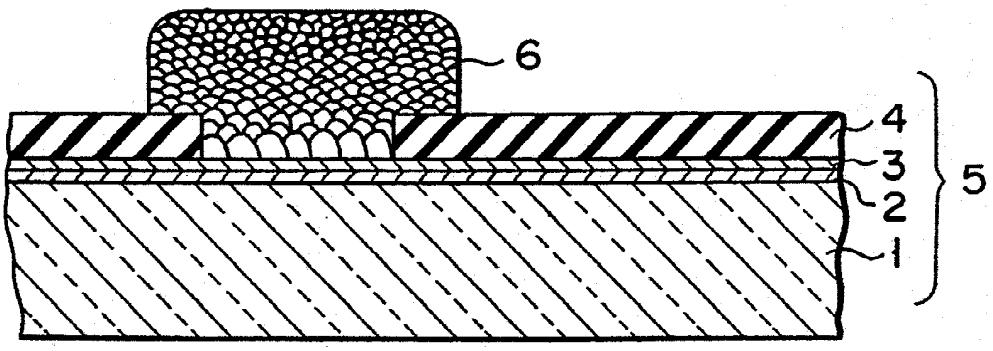


FIG. 1A

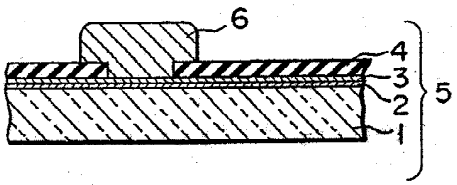


FIG. 1B

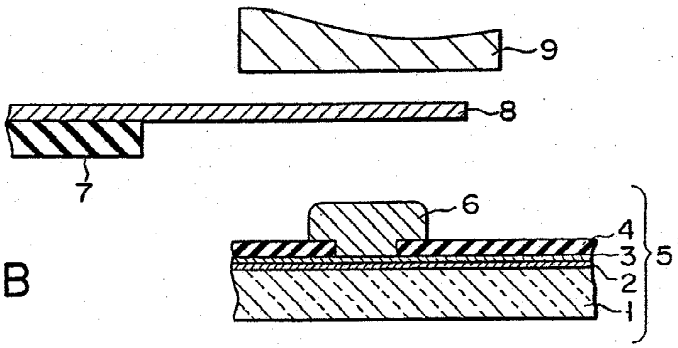
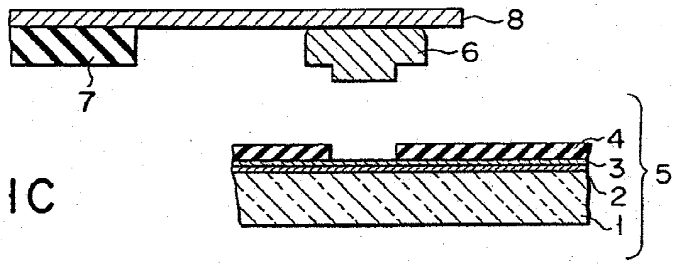


FIG. 1C



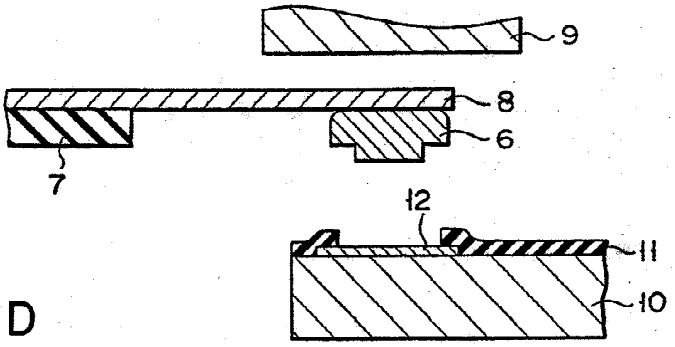


FIG. 1D

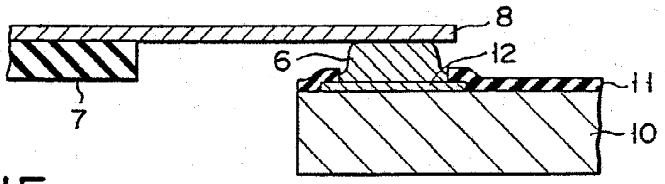


FIG. 1E

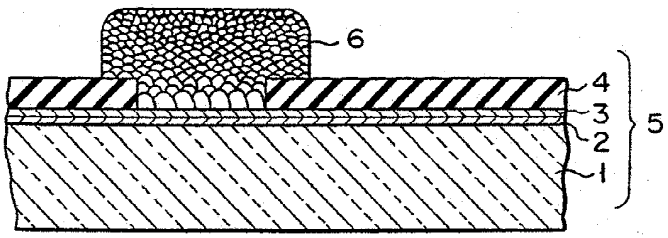


FIG. 2

METHOD OF MANUFACTURING ELECTRONIC PARTS INCLUDING TRANSFER OF BUMPS OF LARGER PARTICLE SIZES

This application is a continuation of application Ser. No. 064,397, filed on June 22, 1988, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to a method of manufacturing electronic parts, based on the transferred bump process.

Recent efforts aimed at miniaturizing a semiconductor chip used in, for example, an IC, LSI, etc., have been accompanied by efforts to reduce the size of its package. The package has a role of an electrode lead to extend from an aluminium electrode on the semiconductor chip, thereby to allow for its easy handling and to protect it from external pressure. The extending of a lead from the aluminium electrode of the semiconductor chip to the terminal of the package can be conveniently effected by use of the tape automated bonding (TAB) process.

The TAB process consists in forming a bump on the electrode and effecting connection between the bump and the electrode lead. It is necessary to use electroplating in order to mount an Au bump on the Al electrode of the semiconductor substrate. However, since it is difficult to directly adhere an Au bump to an Al electrode, the customary process is to deposit a multiple barrier metal mass composed of, for example, Cu, Cr and Ti on the Al electrode, before performing plating.

As a result, a bump-transferring process has been devised which comprises the steps of first forming a bump on a substrate, transferring the bump to a lead, and then to the desired electrode, and thermally pressing the bump to effect the connection with the electrode (Japanese Patent Disclosure Nos. 57-152147 and 60-92648). This proposed process dispenses with the aforementioned barrier metal, thereby simplifying the formation of the bump and the bump assembly, and enabling a plurality of electrodes to be simultaneously connected to terminals.

FIGS. 1A to 1E show the sequential steps of the bump-transferring process. As is shown in FIG. 1A, substrate 5 on which a bump is to be formed is constructed by laminating conductive layer 2, conductive oxide layer 3, and resist pattern 4, in that order, on base-substrate 1. Bump 6 is electroplated in the bump-forming opening of substrate 5. Conductive oxide layer 3 should preferably be prepared from a material which can be readily connected to gold bump 6 and easily released from bump 6 when it is transferred to the lead. In the second step, (FIG. 1B), electrode lead member 8, supported on insulating film 7, is placed on bump 6. Thereafter, heated bonding tool 9 is pressed on electrode lead member 8, thereby transferring bump 6 to electrode lead 8 (FIG. 1C). Later, as can be seen in FIG. 1D, bump 6 transferred to electrode lead 8 is positioned above al electrode (bonding pad) 12 exposed out of passivation layer 11 of semiconductor chip 10. Thereafter, previously heated bonding tool 9 is pressed on electrode lead 8, thereby connecting electrode lead 8 to Al electrode 12, with bump 6 interposed therebetween.

However, the above-mentioned bump-transferring process has drawbacks in that the bump tends to peel off from an oxide layer, to which it is adhered, during the step of electroplating the bump on the substrate and also during the subsequent bump-washing step, thus resulting in a decline in throughput.

SUMMARY OF THE INVENTION

This invention is intended to provide a method of manufacturing electronic parts, based on a bump-transferring process which prevents a bump from falling off during the electroplating and washing steps, and ensures a high bonding strength between the transferred bump and the electrode section of a semiconductor chip.

To attain the above-mentioned object, the present invention provides a bump in which the metal particles in that portion of a bump contacting a substrate are of a larger size than those which are not brought into contact with the substrate.

It is preferable, from the viewpoint of manufacturing, that the particles in that portion of a bump contacting a substrate have a diameter larger than 1 μm, that the bump have a thickness of 15~25 μm, and that the portion of a bump which is composed of the particles having a larger diameter has a thickness of less than 2 μm. The bump can be prepared from gold, copper, etc.

In order to form a bump having the above-defined particle size distribution, it is advisable to set the initial electroplating current density at 2 to 5 times that which is applied thereafter. Either cyanide solution ($KAu(CN)_2$ etc.) or non-cyanide solution ($Na_3Au(SO_4)_2$ etc.) can be used for the plating solution.

The present invention offers the advantages in that the particles in that portion of a bump which contacts a substrate are of a larger size than those which do not contact the substrate, thereby ensuring a stronger adhesive bond between the bump and substrate, and enabling the bump to be readily removed from the substrate when it is to be transferred to the electrode lead, and thus ensuring a high-strength bond between the bump and the electrode section of the semiconductor chip, due to the surface of the removed bump being free from irregularities.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 1E show the sequential steps of manufacturing an electronic part, by use of the bump-transferring method; and

FIG. 2 is a sectional view of the bump embodying the present invention, which has been completely plated.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Example 1

Cr conductive layer 2, having a thickness of 1000 Å, and ITO (Indium Tin Oxide; $InSnO_2$) conductive oxide layer, having a thickness of 2000 Å, were thermally deposited on glass base-substrate 1, in that order. Later, resist pattern 4 acting as a mask, wherein a bump-forming region was perforated, was formed on ITO layer 3 by means of photoetching, thereby completing substrate 5. Thereafter, substrate 5 was overturned so as to form a uniform plating layer, and was dipped, in this state, in a gold-electroplating cyanide solution (65° C., stirred at any time). Electroplating was performed for 30 seconds, with the initial current density increased to 3 times the generally recommended level of 1 A/dm^2. Electroplating then continued under the abovementioned recommended level. This resulted in gold bump 6 being formed with a thickness of 25 μm (FIG. 1A).

When observation was made of the vertical section of bump 6, a crystal particle size distribution such as that indicated in FIG. 2 was observed; i.e. the crystals contacting ITO layer 3 had a particle size larger than 1 μm. The crystals lying thereon, namely, those which do not contact ITO layer 3, had a particle size of about 5000 Å.

As is indicated in FIG. 1B, copper electrode lead 8, supported by polyimide film 7 and plated with tin, was set above bump 6. Electrode lead 8 was pressed on bump 6 by means of bonding tool 9 heated to 280° C. for 2 seconds, under the pressure of 20 g per Pin (lead number). Later, bonding tool 9 was removed and electrode lead 8 was peeled off from substrate 5, thus enabling bump 6 to be transferred to electrode lead 8, as can be seen in FIG. 1C.

Later, as is shown in FIG. 1D, transferred bump 6 was set above Al electrode (bonding pad) 12 exposed out of passivation layer 11 of semiconductor chip 10, and bonding tool 9 was positioned above electrode lead 8. Using bond tool 9, bump 6 was thermally pressed onto Al electrode 12 for 2 seconds, at a temperature of 380° C., under the pressure of 80 g for 1 Pin. As is shown in FIG. 1E, electrode 8 was connected to Al electrode 12, with bump 6 interposed therebetween. The bonding strength between bump 6 and Al electrode 12 indicated 40 g/lead.

When a bump is formed by the above-mentioned process, the surface of ITO layer 3 is activated because the initial current density is high, and the metal particles impinge on ITO layer 3 at a high speed, thus presumed to increase bonding strength.

Example 2

Electroplating was applied for 3 seconds to a substrate on which a bump was to be formed, with the initial current density increased to 5 times the generally recommended level of 1 A/dm^2. Subsequently, electroplating was continued at this recommended level. Then, as is indicated in FIG. 2, a gold bump 6 was formed on the substrate 5, in such a manner that the portion of the bump contacting the substrate consisted of particles larger than those in other portions thereof. It was confirmed that use of the above method effectively prevented the bump formed thereby from peeling off from or falling off the substrate.

Control

A bump was formed on a substrate substantially in the same manner as in Example 1, except that electroplating was performed with the generally recommended current level of 1 A/dm^2 being sustained throughout the process. The bump thus formed was connected to the Al electrode section of a semiconductor chip. Observation of the vertical section of an electroplated gold bump showed that the crystal particles of the bump all had a diameter of about 5000 Å, thereby indicating that this method failed to produce a distribution of crystal particle diameters such as was obtained in Examples 1 and 2.

In this Control, the bump either peeled off from fell off the substrate during the electroplating step and the succeeding washing step. The bonding strength between the bump and Al electrode was found to be 10 g/lead.

It should be noted that the present invention is not limited to the above-mentioned examples. Any other method of forming a bump is applicable, provided that the bump is prepared in such a manner that those portions of a bump which contact the substrate are formed of larger crystal particles than the other portions thereof.

What is claimed is:

1. A method of manufacturing electronic parts, comprising:

a first step of forming on the surface of a substrate a bump with substantially all the metal crystal particles of that portion of the bump which contacts the surface of the substrate having larger diameters than the metal crystal particles of that portion of the bump which does not contact the surface of the substrate;

a second step of transferring the bump to an electrode lead; and

a third step of connecting an electrode lead to the predetermined electrode section of the semiconductor chip, by means of the transferred bump.

2. The method according to claim 1, wherein the metal crystal particles of that portion of the bump which contacts the substrate have a diameter larger than 1 μm.

3. The method according to claim 1, wherein the bump is formed by electroplating.

4. The method according to claim 3, wherein the initial current density of electroplating applied to the formation of a bump is defined to be 2–5 times the current density which is used thereafter.

5. The method according to claim 1, wherein the bump has a thickness of 15–25 μm.

6. The method according to claim 1, wherein the bump is prepared from gold or copper.

7. The method according to claim 1, wherein the substrate on which the bump is to be formed is constructed by laminating a conductive layer and conductive oxide layer, in that order, on the basesubstrate.

8. The method according to claim 7, wherein the base-substrate is prepared from glass, the conductive layer from chromium, and the conductive oxide layer from ITO.

9. The method according to claim 1, wherein the layer composed of the metal crystal particles having a larger diameter has a thickness of less than 2 μm.

* * * * *

EXHIBIT DD

United States Patent [19]

Yorikane

Best Available Copy

[11] **4,263,606**

[45] **Apr. 21, 1981**

[54] **LOW STRESS SEMICONDUCTOR DEVICE LEAD CONNECTION**

[75] Inventor: **Masaharu Yorikane, Tokyo, Japan**

[73] Assignee: **Nippon Electric Co., Ltd., Japan**

[21] Appl. No.: **925,324**

[22] Filed: **Jul. 17, 1978**

[30] **Foreign Application Priority Data**

Jul. 18, 1977 [JP] Japan 52/86524

[51] **Int. Cl.**[3] **H01L 23/48; H01L 29/46; H01L 29/54**

[52] **U.S. Cl.** **357/71; 357/65; 357/67; 357/68**

[58] **Field of Search** 357/65, 67, 71, 72, 357/68

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4,060,828	11/1977	Satonaka	357/71

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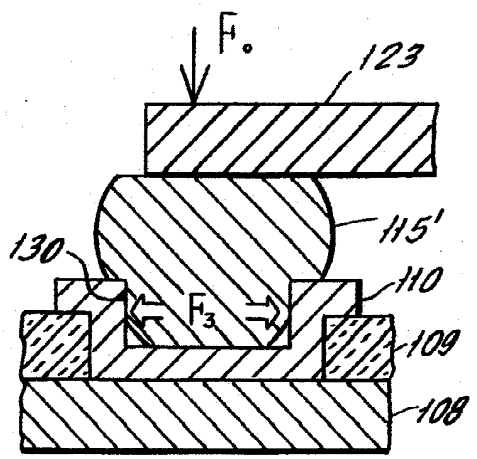
IBM Technical Disclosure Bulletin; by Ainslie, vol. 11, No. 10, Mar. 1969, p. 1339.

Primary Examiner—Andrew J. James

[57] **ABSTRACT**

An external connection structure for an integrated semiconductor device is disclosed. The semiconductor device includes a substrate on which a wiring layer, which is covered by an insulator layer is disposed. According to the invention, an aperture is provided in the insulative layer to expose the wiring layer. A metallic film lines the aperture, covering the exposed portion of the wiring layer and defining a recess. A bump type electrode of a malleable metal is disposed in the recess. The bump electrode is spaced from the side walls of the recess, and projects beyond the surface of the metallic film surrounding the recess for connection under pressure with an external lead plate.

5 Claims, 15 Drawing Figures



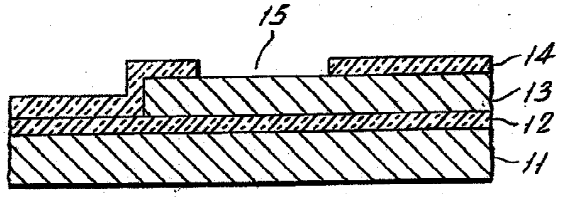


FIG. 1a
PRIOR ART

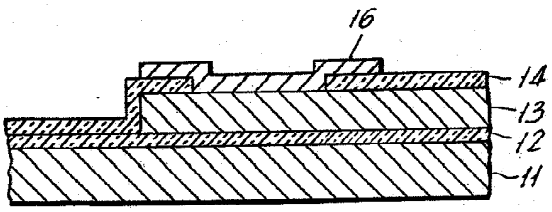


FIG. 1b
PRIOR ART

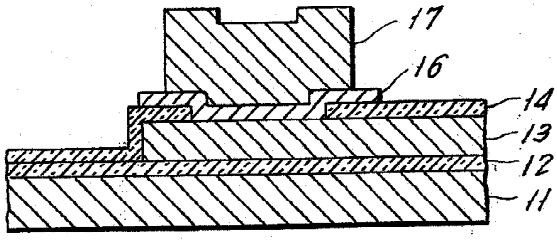


FIG. 1c
PRIOR ART

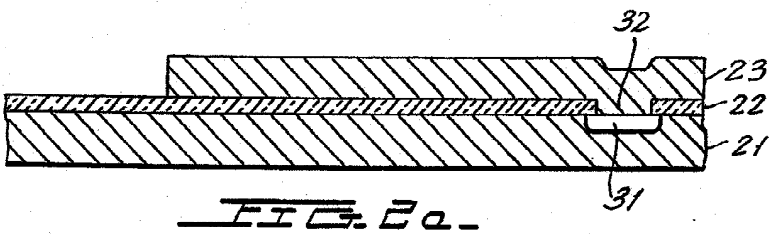


FIG. 2a

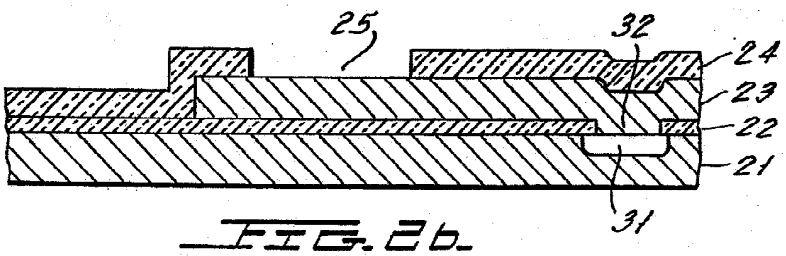


FIG. 2b

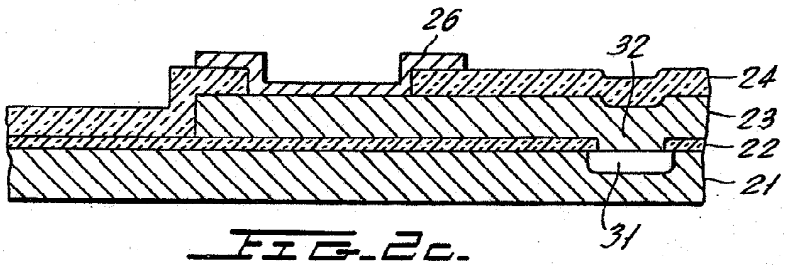


FIG. 2c

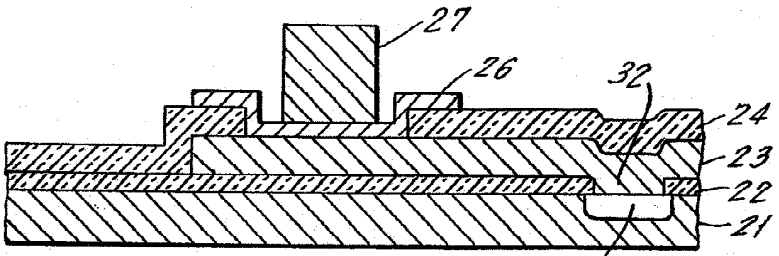


FIG. 2d

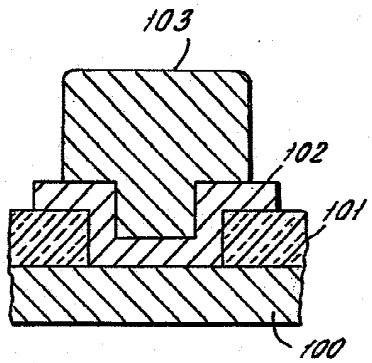


FIG. 3a.
PRIOR ART

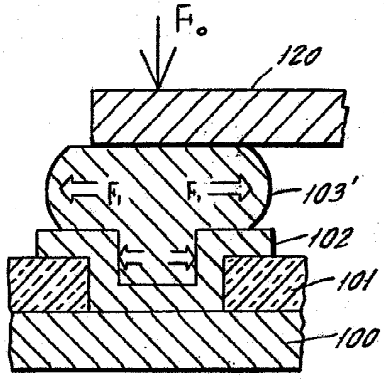


FIG. 3b.
PRIOR ART

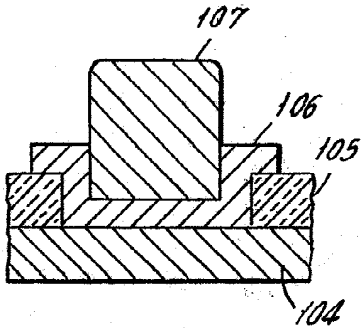


FIG. 4a.
PRIOR ART

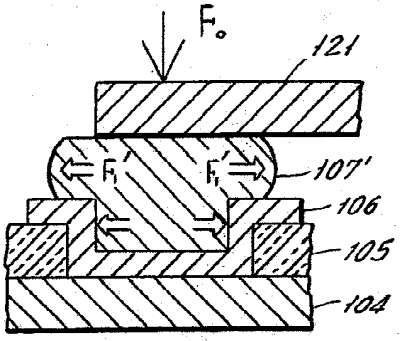


FIG. 4b.
PRIOR ART

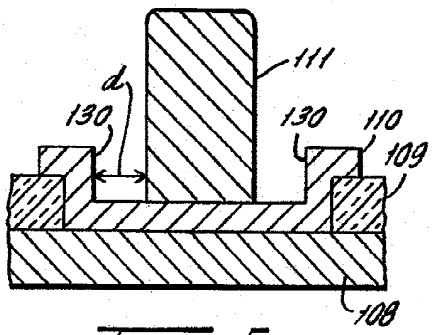


FIG. 5a

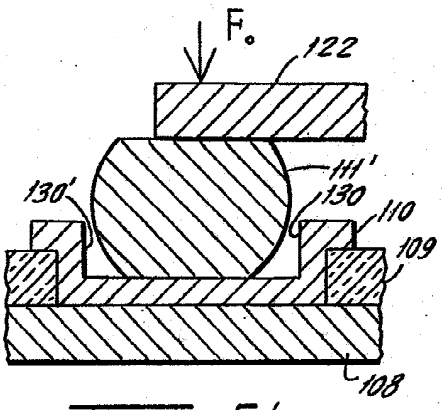


FIG. 5b

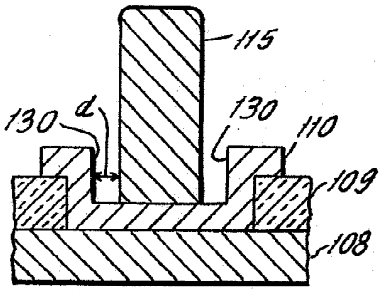


FIG. 6a

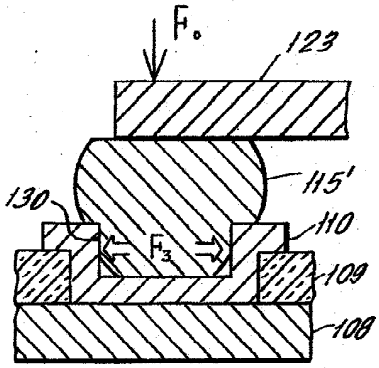


FIG. 6b

LOW STRESS SEMICONDUCTOR DEVICE LEAD CONNECTION

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device, and more particularly, to a semiconductor device in which metallic protrusions (hereinafter called "bumps") are provided at an electrode wiring section on a semiconductor chip to make electrical connection with external leads.

Heretofor, electrodes have been formed on a semiconductor chip with a silicon substrate or the like in the following manner. After required circuit elements are formed in a semiconductor chip and the surface of the chip is covered with an insulator film (for example, a silicon oxide film), the insulator film is partially removed by etching at portions where electrical connection to regions of semiconductor chip is required to form apertures. Then, aluminum is deposited over the surface of the chip including the apertures and is partially removed by etching to form a predetermined pattern of wirings. At portions of the wirings where external leads are to be connected, a thin film of titanium, platinum or the like is formed and bumps of highly conductive metal such as gold, silver or the like are formed thereon by plating. The external leads are connected to the bumps by thermo-compression bonding. The intermediate thin film of titanium or platinum is necessary, because if the gold bumps are directly contacted with the aluminum layer without the intermediate thin film, then an alloy layer called "purple plague" would be formed therebetween by chemical reaction between aluminum and gold and cracks would arise therebetween due to volume increment by formation of this alloy which would result in anomalous increase in a resistance or breaking of a circuit.

Various proposals have been made for connection between external leads and bumps, and one of them is disclosed in British Pat. No. 1,196,834. According to this disclosure, aluminum electrodes making electrical contact with operating regions of a semiconductor chip are formed extending onto an oxide film outside of the operating region, and then at an end of the aluminum electrode, a layer of refractory metal such as titanium, chromium, or tungsten, serving as a barrier film for preventing formation of the purple plague is formed so as to overlap the end of the aluminum electrode. Thereafter an oxide film is formed over the surface of the chip, and the predetermined part of the oxide film on the refractory metal layer is selectively removed by etching to make an aperture in which the refractory metal is exposed. A conductive metal layer of conductive metal liable to be wetted with solder (tin-lead alloy), such as a layer of nickel, copper or gold is formed within the aperature. Thereafter, the whole chip is immersed in a solder bath to form a bump of solder on the conductive metal layer within the aperture.

The bump thus formed is in contact with the inner wall of the oxide layer in the aperture. Therefore upon thermo-compression bonding an external lead to the bump, the bump would be deformed by the mechanical force exerted thereon due to the thermo-compression bonding, and it is liable to occur that cracks are produced in the oxide film or the oxide film is torn off around the bump due to the stress associated with the deformation. Consequently, humidity and contamination would enter from external atmosphere into the semiconductor device through the cracks or the torn portions and would corrode the conductive metal as well as the aluminum wiring, which causes accidents such as poor connection or breaking of a circuit or degradation of electrical performances of the device.

According to another proposal in the prior art such as disclosed, for example, in U.S. Pat. No. 3,942,187, an aluminum wiring layer is provided extending from an operating region of a chip onto a first oxide film, and further, a first nickel layer is formed on the oxide film so as to overlap the end of the aluminum wiring layer. Thereafter, a second oxide film layer is formed over the entire surface of the chip and is partially removed from a portion on the first nickel layer to provide an aperture where a second nickel layer is formed within the aperture as well as on the peripheral portion of the aperture. A bump of copper or gold is provided on the second nickel layer so as to cover the aperture. However, even with this structure, the bump would be deformed laterally, when an external lead is bonded thereto, by the pressure exerted upon the bonding, and consequently cracks or tear-off would arise in the second oxide film layer located around the deformed bump due to the stress associated with the deformation. Therefore, it is inevitable that the reliability of the semiconductor device is greatly lowered.

BRIEF SUMMARY OF THE INVENTION

It is a primary object of the present invention to provide a semiconductor device having an excellent reliability in which, upon bonding an external lead to a bump formed on a semiconductor chip, generation of cracks and tears of an insulator film caused by a mechanical pressure exerted upon the bump can be prevented.

The semiconductor device according to the present invention is characterized in that a metallic bump has a smaller area than that of a recess made by an aperture of an insulator film at the intended connecting portion of an internal wiring layer and is formed within the recess remote to the inner wall of the recess.

According to the present invention, when external leads are bonded to the metallic bumps provided on or above the connecting portions of the internal metallic wiring on a semiconductor chip, thermo-compression bonding and the bumps are deformed by a mechanical pressure associated with the bonding operation, a stress associated with deformation of the bumps would not be applied directly to the insulator film, because the metallic bumps and the recess made by aperture of the insulator film are located separately from each other. In order words, the separation gap between the insulator film and the bump allows the deformation of the bump caused by the bonding operation and the stress is absorbed by the bump inself and is not transmitted to the insulator film. Consequently, cracks are not generated in the protective film and the protective film is not torn. The connection with the external leads can be effected reliably without deteriorating the protective effect of the film, so that it is possible to provide a semiconductor device having an excellent reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1(*a*) to 1(*c*) are cross-sectional views showing a bump portion of a prior art semiconductor device in successive steps of the formation of the bump;

FIGS. 2(*a*) to 2(*d*) are cross-sectional views showing a semiconductor device according to one preferred embodiment of the present invention in successive steps of the formation of the bump;

FIGS. 3(*a*) and 4(*a*) are cross-sectional views showing bump structures of semiconductor devices in the prior art, and FIGS. 3(*b*) and 4(*b*) are cross-sectional views showing deformation of the bumps shown in FIGS. 3(*a*) and 4(*a*), respectively, when a mechanical pressure is applied to the bumps;

FIG. 5(*a*) is a cross-sectional view showing the bump structure of the semiconductor device according to one preferred embodiment of the present invention, and FIG. 5(*b*) is a cross-sectional view showing deformation of the bump structure shown in FIG. 5(*a*) when a mechanical pressure is applied to the bump; and

FIG. 6(*a*) is a cross-sectional view showing an undesirable mode of embodiment of the bump structure of the semiconductor device, and FIG. 6(*b*) is a cross-sectional view showing deformation of the bump structure shown in FIG. 6(*a*) when a mechanical pressure is applied to the bump.

DETAILED DESCRIPTION OF THE INVENTION

The semiconductor device of the prior art has the structure illustrated in FIGS. 1(*a*) to 1(*c*). A silicon substrate **11** covered with a first protective film **12** of silicon dioxide is prepared, in which desired circuit elements are formed. An aluminum wiring layer **13** is formed on the film **12** and a second protective film **14** of silicon dioxide is deposited on the first protective film **12** and the wiring layer **13**. An aperture **15** is opened in the second film **14** at a portion where a bump **17** is to be formed, as shown FIG. 1(*a*). A barrier layer **16** of a refractory metal is formed successively within the aperture **15** and on the second film **14** at the periphery of the aperture **15**, as shown in FIG. 1(*b*). Then a bump **17** which is registered in position with the aperture **15** and has a bottom area larger than the area of the aperture **15** or the area of the recess of the film **16** is formed on the barrier layer **16** (FIG. 1(*c*)). When this bump **17** and an external lead (not shown) are bonded together through a thermo-compression bonding process, a mechanical pressure is applied to the top surface of the bump **17**, so that a concentrated stress associated with this mechanical pressure is impressed upon the bottom portion of the bump **17** in contact with the protective metal **16**. This mechanical pressure causes the protective film **14** to widen the aperture **15**. Due to this stress, the protective film **14** about the portion right under the end portion of the bump **17** is liable to be destroyed or torn, and external humidity and contamination would enter into the device through the destroyed or torn portion and would deteriorate the electrical characteristics and corrode the aluminum wiring path **13**, so that the semiconductor devices of the above-described type in the prior art had extremely undesirable shortcomings in reliability.

In order to eliminate such shortcomings, the present invention provides a novel structure of a semiconductor device illustrated in FIGS. 2(*a*) to 2(*d*) as one preferred embodiment of the invention.

Referring to FIG. 2(*a*), a semiconductor substrate **21** such as silicon substrate covered with an electrically insulating film **22** of, e.g., silicon dioxide is prepared, in which desired circuit elements are formed. An internal wiring layer **23** is formed on the insulating film **22**, one end of which is connected to an operating region **31** of the substrate **21** through an aperture **32** of the insulating film **22**. As a material of the wiring layer **23**, aluminum is typically employed and a pattern of the wiring layer **23** is formed by an etching process. Then over the surface of the substrate **21** including the wiring layer **23** is formed a protective insulator film **24** by vapor deposition, and thereafter, a desired aperture **25** is provided by etching at a portion where a bump is to be formed as shown in FIG. 2(*b*). As the protective film **24**, normally a silicon di-oxide film is used for the purpose of preventing the wiring layer **23** from corrosion and mechanical damage, and the thickness of the protective film **24** is about 5000 Å in this example. Subsequently, a proTective metal layer (barrier layer) **26** of a refractory metal such as molybdenum, tantalum, tungsten chromium, or titanium is formed on the exposed portion of the wiring layer **23** in the aperture **25** and on the protective film **24** at the periphery of the aperture **25** for preventing the formation of the purple plague, which is caused by mutual diffusion of aluminum of the wiring path **23** and gold of a bump, as shown in FIG. 2(*c*). In general, the protective metal layer **26** is hardly etched because its etching speed by the chemical ethant is low. Therefore, a lift-off process is favorably employed for forming the pattern thereof. Subsequently, a bump **27** is so formed, as shown in FIG. 2(*d*), that the bump **27** is positioned within the aperture **25** and within the recess of the layer **26** made by the aperture without contacting with the inner peripheral sides of the recess and has a smaller bottom area which is contacted with the surface of the protective metal layer **26** than the area of any of the aperture **25** and the recess.

When an external lead (not shown) is bonded to the bump **27** of the above-described structure by a thermocompression or other bonding method applying a mechanical pressure to the bump **27**, the bump **27** is deformed by a mechanical pressure and the stress is then concentrated at the bottom edge of the bump **27** in contact with the protective metal layer **26** but not applid to the protective film **24** due to a gap between the inner peripheral side surface of the aperture **25** or the recess and the bump **27**. In other words, the mechanical pressure generated upon bonding can be absorbed by the bump **27** itself and therefore, the protective film **24** would never be applied with such an excessive pressure that it may be either destroyed or torn due to the pressure. Consequently, even if the bump **27** and an external lead are connected under a mechanical pressure, the protective film **24** retains its normal protection effect, and a semiconductor device having a high reliability can be obtained.

The height of the bump **27** is about 20 μm in the example, and favourably the bump **27** is formed of gold by plating. In this case, photo-resist mask is deposited to cover the semiconductor chip except for the location where the bump **21** is to be formed, and the bump **27** is formed by electroplating. On the other hand, the protective metal layer **26** serves to protect the aluminum internal wiring **23** within the aperture **25**, and also, in case where the bump **27** and the internal wiring **23** are made of different metals as is the case of the above-described embodiment (aluminum-gold), it serves to prevent mutual diffusion therebetween. The thickness of the protective metal layer **26** is about 2000 Å in this example.

Now, in order to further clarify the effects of the semiconductor device according to the present inven-

tion, description will be made with reference to FIGS. 3 to 6.

Cross-sectional views illustrating bump structures in the prior art are shown in FIGS. 3(*a*) and 4(*a*), in which a predetermined portion of a silicon oxide protective films **101** and **105** corresponding to the second protective film **14** shown in FIGS. 1(*a*) to 1(*c*) on an aluminum internal wiring layers **100** and **104** corresponding to the wiring path **13** shown in FIGS. 1(*a*) to 1(*c*), respectively, are removed by etching, and then a protective metal layers **102** and **106** corresponding to the protective metal layer **16** shown in FIGS. 1(*a*) to 1(*c*) is formed. FIG. 3(*a*) shows a subsequent state where a bump **103** has been formed within an aperture as extended up to the upper surface of the silicon oxide film **101**, while FIG. 4(*a*) shows an alternative subsequent state where a bump **107** has been formed only within the aperture with its side surface kept in contact with an inner peripheral side surface of the protective film **106** in the aperture in the silicon oxide film **105**. When the bumps **103** and **107** are connected with an external lead **120** and **121** as shown in FIGS. 3(*b*) and 4(*b*), under a mechanical pressure Fo by a thermo-compression bonding process, the bump **103'** and **107'** will be deformed by the mechanical pressure Fo applied to the top surface of the bumps **103'** and **107'**, and the stress associated with this deformation is applied to both the protective metal layers **102** and **106** and to the silicon oxide films **101** and **105**, respectively.

The external leads **120** and **121** are made of copper and plated with gold or silver. They are respectively placed on the top surface of the bumps **103** and **107**. Thereafter, the mechanical pressure Fo is supplied on the top surface of the external leads **120**, **121** to connect the bump **103'** to the lead **120** and the bump **107'** to the lead **121**. In this process, the value of the mecanical pressure Fo needs about 1,000 kg/cm^2 in the temperature range from 400° C. to 500° C.

As will become apparent by comparing FIGS. 3(*a*)and 4(*a*) with FIGS. 3(*b*) and 4(*b*), respectively, prior art bumps **103'** largely deformed in the lateral directions on the protective metal layer **102**, **106** and above the silicon oxide film **101**, **105** by the internal stresses F_1 and F_1'.

The internal stresses F_2 are transmitted to the silicon oxide films **101** and **105** via the protective metal layer **102** and **106**. As a result, cracks and tears arise in the silicon oxide film **101** and **105**.

Even with the bump **107** not formed above the silicon oxide film **105** but formed in contact with the inner side surface of the recess of the protective metal layer **106**, since the pressure F_0 is uniformly applied to the entire bump **107'**, not only the bump **107'** is deformed over the protective metal layer **106** by the internal stress F_1', but also the internal stress F_2' occurs to stress the metal lay **106'** and the silicon oxide film **105** in the lateral directions via the side surface of the recess, that is, via the side surface where the protective metal layer **106** makes contact with the bump **107'**, so that cracks and tears will be also generated in the silicon oxide film **105**.

FIG. 5(*a*) shows a bump structure according to the present invention in which a silicon oxide protective film **109** corresponding to the protective film **24** shown in FIGS. 2(*a*) to 2(*d*) on an aluminum internal wiring layer **108** corresponding to the wiring path **23** shown in FIGS. 2(*a*) to (*d*) is selectively and partly removed to form an aperture, and the recess as separated from inner side surfaces **130** of the protective metal layer **110**. A shown in FIG. 5(*b*), when the bump **111** and an external lead **122** are connected with each other, the bump **111'** is deformed by the mechanical pressure F_0 (about 1000 Kg/cm^2) applied to the top surface of the bump **111'**, but the stress associated with the deformation would not be applid directly to the silicon oxide film **109** through the inner side surfaces **130'** of the protective metal layer **110**, because the deformation occurs only within the aperture. Consequently, connection can be achieved reliably, and cracks and tears are not generated in the protective film **109**, so that a semiconductor device having an extremely high reliability can be provided.

Here, it is to be noted that in the bump structure illustrated in FIG. 5(*a*), the separation distance d between the protective metal side surface **130** and the side surface of the bump **111** could be appropriately varied depending upon the materials and dimensions of the bump **111**, protective metal layer **130** and protective film **109** and upon the magnitude of the mechanical pressure applied during the bonding operation. However, if a separation distance d' between a protective metal layer **110** and a bump **115** is too small as illustrated in FIGS. 6(*a*), then the bump **115** will be deformed as shown in FIG. 6(*b*) by the mechanical pressure F_0 applied thereto beyond the inner edge **230** of the layer **110**, the stress F_3 is transmitted to the protective metal layer **110** and the protective film **109** without being sufficiently mitigated, so that there is a fear that cracks and tears may arise in the protective film **109**. In the case of the construction according to the preferred embodiment shown in FIG. **2**, the separation distance ranging from 3 μm to 15 μm could be provided for the diameter of the recess in the protective metal layer **26** of 100 μm. In other words, the bump has a bottom area as small as 49 to 88 percent of the internal area of the recess.

However, the present invention should not be limited to the above-described embodiment, but the invention is featured by the formation of the bump which is located within the aperture or recess made by the protective film on or above the internal wiring layer and which has a smaller bottom area than the area of any of the aperture and the recess. Furthermore, in such a bump structure, although the sepration distance between the bump and the side surface of the recess is determined by various factors such as the materials and dimensions of the bump, protective metal layer and protective film and the magnitude of the mechanical pressure, the effect of the present invention can be fully achieved, so long as such degree of distance is maintained that the stress associated with the bump deformation caused by the mechanical pressure upon interconnection of the bump with an external lead may be sufficiently mitigated. In this point of view, the bottom area of the bump shall be at most 90% of the inner area of the recess in which the bump is formed. It is of course favorable that the bump is so separated from the inner wall of the recess that the bump is not brought into contact with the inner wall of the recess even by deformation thereof due to mechanical pressure for the bonding.

In addition, while a silicon dioxide film was used as a protective film in the above-described embodiment, other appropriate insulator films such as a silicon nitride film, a glass film, or a combination of these films could be used, and for the protective metal, besides Mo, Ta and W other metals such as Pt, Ti, etc. could be used, so long as the metal can prevent mutual diffusion between the bump of gold and the internal wiring path of alumi-

num. Furthermore, for the bump material, not only gold, but also silver could be employed.

A semiconductor device according to the invention may have a plurality of bumps having the above-described structure on one semiconductor chip, and a plurality of external leads may be bonded to the bumps simultaneously. In particular, many bumps may be simultaneously fabricated in the same process in an LSI device.

What is claimed is:

1. A semiconductor device comprising: a semiconductor substrate; a first insulating film covering at least a portion of said substrate; a wiring path formed on said first insulating film; a second insulating film covering said wiring path; an aperture being provided in said second insulating film, exposing at least a portion of said wiring path; a first protective metal layer entirely covering said portion of said wiring path exposed through said aperture, to form a recess therein; a bump electrode terminal made of a metal provided in said recess on said first metal layer, said bump electrode terminal being in contact with said first metal layer over an area smaller than the area of said recess; said terminal further having a bottom surface, a top surface and a side surface; said bump electrode terminal protruding from said recess beyond said first protective metal layer; and an external lead plate having an end portion which has been connected to said top surface of said bump electrode terminal by means of mechanical pressure in such a manner that said side surface of said bump electrode terminal has been deformed laterally toward said first protective metal layer said terminal further having a bottom surface, said side surface being entirely separated from said first protective metal layer except where said side and bottom surfaces meet.

2. A semiconductor device as claimed in claim 1, wherein a metal different from said metal of said bump electrode terminal forms said wiring path.

3. A semiconductor device as claimed in claim 1, wherein said bottom surface of said recess has a bottom surface, and wherein said bump electrode terminal has an area not more than 90% the area of said bottom surface of said recess.

4. A semiconductor device comprising: a semiconductor substrate including a plurality of circuit elements therein; an aluminum internal wiring path formed on said semiconductor substrate and electrically connecting said circuit elements to form a predetermined circuit; a silicon oxide film formed at least on said aluminum internal wiring path; an aperture provided in a predetermined portion of said silicon oxide film, exposing at least a portion of said internal wiring path; a metallic film formed to cover said aperture entirely, to form therein a recess having a peripheral wall, said metallic film being formed of a metal selected from the group consisting of molybdenum, tantalum, tungsten, platinum and titanium; and a gold protrusion formed on said metallic film within said aperture, said gold protrusion being separated from said peripheral surface of said recess; said gold protrusion projecting beyond the surface of said metallic film and having a top surface for connection under pressure with an external lead plate.

5. A semiconductor device as claimed in claim 4, wherein said gold protrusion covers at most 90 percent of the bottom area of said recess.

* * * * *

EXHIBIT EE

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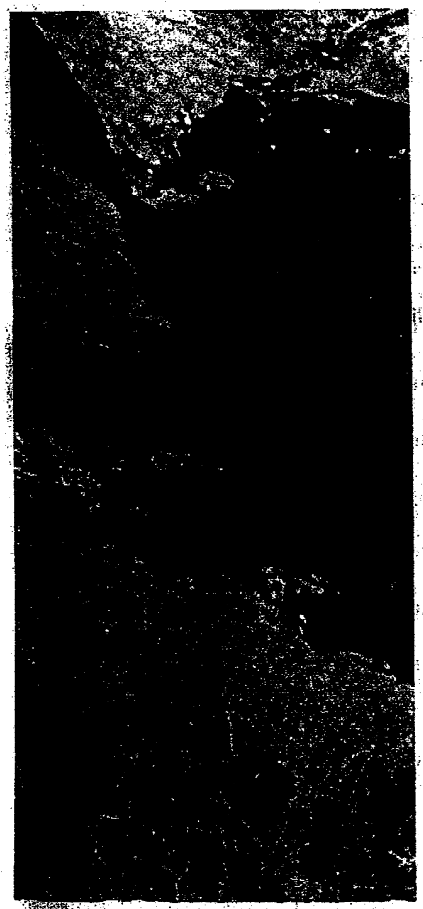
Fourth Edition



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On the cover: Pattern produced from white light by a computer-generated diffraction plate containing 529 square apertures arranged in a 23 × 23 array. (R. B. Hoover, Marshall Space Flight Center)

On the title pages: Aerial photograph of the Sinai Peninsula made by Gemini spacecraft. (NASA)

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pactamycin [MICROBIO] An antitumor and antibacterial antibiotic produced by *Streptomyces pactum* var. *pactum*. { ˌpak·tə'mīs·ən }

pad [AERO ENG] *See* launch pad. [ANAT] A small circumscribed mass of fatty tissue, as in terminal phalanges of the fingers or the underside of the toes of an animal, such as a dog. [ELECTR] **1.** An arrangement of fixed resistors used to reduce the strength of a radio-frequency or audio-frequency signal by a desired fixed amount without introducing appreciable distortion. Also known as fixed attenuator. **2.** *See* terminal area. [ENG] **1.** A layer of material used as a cushion or for protection. **2.** A projection of excess metal on a casting forging, or welded part. **3.** A takeoff or landing point for a helicopter or space vehicle. [MET] The brickwork that is beneath the molten iron at the base of a blast furnace. { pad }

pad deluge [AERO ENG] Water sprayed on certain launch pads during rocket launching in order to reduce the temperatures of critical parts of the pad or the rocket. { 'pad 'delˌyüj }

padder [ELECTR] A trimmer capacitor inserted in series with the oscillator tuning circuit of a superheterodyne receiver to control calibration at the low-frequency end of a tuning range. { 'pad·ər }

padding [COMPUT SCI] The adding of meaningless data (usually blanks) to a unit of data to bring it up to some fixed size. { 'pad·iŋ }

paddle [AERO ENG] A large, flat, paddle-shaped support for solar cells, used on some satellites. [DES ENG] Any of various implements consisting of a shaft with a broad, flat blade or bladelike part at one or both ends. { 'pad·əl }

paddle wheel [MECH ENG] **1.** A device used to propel shallow-draft vessels, consisting of a wheel with paddles or floats on its circumference, the wheel rotating in a plane parallel to the ship's length. **2.** A wheel with paddles used to move leather in a processing vat. { 'pad·əl ˌwēl }

paddle-wheel steamer [NAV ARCH] A steamer propelled by a wheel or wheels having long paddles, some of which are curved and feathering; the wheel revolves in a vertical plane parallel to the length of the ship; one type of craft has a wide stern wheel, and the other type has two narrow side wheels. { 'pad·əl ˌwēl ˌstēm·ər }

pad dyeing [TEXT] A process in which fabrics are dyed by passing them between rollers. { 'pad ˌdī·iŋ }

Padé table [MATH] A table associated to a power series having in its pth row and qth column the ratio of a polynomial of degree q by one of degree p so that this fraction expanded into a power series agrees with the original up to the $p + q$ term. { 'pād·ā ˌtā·bəl }

padlock [DES ENG] An unmounted lock with a shackle that can be opened and closed; the shackle is usually passed through an eye, then closed to secure a hasp. { 'padˌläk }

padparadsha *See* orange sapphire. { pad'par·ədˌshä }

paedogamy [INV ZOO] A type of autogamy in certain protozoans whereby there is mutual fertilization of gametes derived from a single cell. { pē'däg·ə·mē }

paedomorphosis [EVOL] Phylogenetic change in which adults retain juvenile characters, accompanied by an increased capacity for further change; indicates potential for further evolution. { ˌpēd·ə'mȯr·fə·səs }

Paenungulata [VERT ZOO] A superorder of mammals; including proboscideans, xenungulates, and others. { ˌpēn,əŋ·gyə'lād·ə }

Paeoniaceae [BOT] A monogeneric family of dicotyledonous plants in the order Dilleniales; members are mesophyllic shrubs characterized by cleft leaves, flowers with an intrastaminal disk, and seeds having copious endosperm. { ˌpē·ə·nē'ās·ē,ē }

paesa [METEOROL] A violent north-northeast wind of Lake Garda in Italy. { pī'ā·zə }

paesano [METEOROL] A northerly night breeze, blowing down from the mountains, of Lake Garda in Italy. { pī'zä·nō }

page [COMPUT SCI] **1.** A standard quantity of main-memory capacity, usually 512 to 4096 bytes or words, used for memory allocation and for partitioning programs into control sections. **2.** A standard quantity of source program coding, usually 8 to 64 lines, used for displaying the coding on a cathode-ray tube. { pāj }

pageable memory [COMPUT SCI] The part of a computer's main storage that is subject to paging in a virtual storage system. { 'pāj·ə·bəl 'mem·rē }

page data set [COMPUT SCI] A file for storing images of pages in a virtual storage system, so that they can be returned to main storage for further processing when needed. { 'pāj 'dad·əˌset }

page boundary [COMPUT SCI] The address of the first (lowest) word or byte within a page of memory. { 'pāj ˌbaún·drē }

page fault [COMPUT SCI] An interruption that occurs while a page which is referred to by the program is being read into memory. { 'pāj ˌfȯlt }

page printer [COMMUN] A high-speed printer used to transpose messages received on paper tape to full-page format, by printing characters one at a time. [COMPUT SCI] A computer output device which composes a full page of characters before printing the page. { 'pāj ˌprint·ər }

page proof [GRAPHICS] A proof received from a compositor after the galley, and having the form of the final page, usually including any illustrations. { 'pāj ˌprüf }

pager [COMMUN] A receiver in a radio paging system. { 'pāj·ər }

page reader [COMPUT SCI] In character recognition, a character reader capable of processing cut-form documents of varying sizes; sometimes capable of reading information in reel forms. { 'pāj ˌrēd·ər }

page skip [COMPUT SCI] A control character that causes a printer to skip over the remainder of the current page and move to the beginning of the following page. { 'pāj ˌskip }

page table [COMPUT SCI] A key element in the virtual-memory technique; a table of addresses where entries are adjusted for easy relocation of pages. { 'pāj ˌtā·bəl }

Paget's cells [PATH] Large, epithelial cells with clear cytoplasm found in certain breast and skin cancers. { 'paj·əts ˌselz }

Paget's disease [MED] **1.** A type of carcinoma of the breast that involves the nipple or areola and the larger ducts, characterized by the presence of Paget's cells. **2.** Osseous hyperplasia simultaneous with accelerated deossification. **3.** An apocrine gland skin cancer, composed principally of Paget's cells. { 'paj·əts dē,zēz }

page turning [COMPUT SCI] **1.** The process of moving entire pages of information between main memory and auxiliary storage, usually to allow several concurrently executing programs to share a main memory of inadequate capacity. **2.** In conversational time-sharing systems, the moving of programs in and out of memory on a round-robin, cyclic schedule so that each program may use its allotted share of computer time. { 'pāj ˌtərn·iŋ }

pagination [GRAPHICS] The art of planning page format to allow sequence page numbering. { ˌpaj·ə'nā·shən }

paging [COMPUT SCI] The scheme used to locate pages, to move them between main storage and auxiliary storage, or to exchange them with pages of the same or other computer programs; used in computers with virtual memories. { 'pāj·iŋ }

paging rate [COMPUT SCI] The number of pages per second moved by virtual storage between main storage and the page data set. { 'pāj·iŋ ˌrāt }

paging system [COMMUN] A system which gives an indication to a particular individual that he is wanted at the telephone, such as by sounding a number on musical gongs, calling by name over a loudspeaker, or producing an audible signal in a radio receiver carried in the individual's pocket. { 'pāj·iŋ ˌsis·təm }

pagoda stone [GEOL] **1.** A Chinese limestone showing in section fossil orthoceratites arranged in pagodalike designs. **2.** An agate whose markings resemble pagodas. { pə'gōd·əˌstōn }

pagodite *See* agalmatolite. { 'pag·əˌdīt }

Paguridae [INV ZOO] The hermit crabs, a family of decapod crustaceans belonging to the Paguridea. { pə'gyür·əˌdē }

Paguridea [INV ZOO] A group of anomuran decapod crustaceans in which the abdomen is nearly always asymmetrical, being either soft and twisted or bent under the thorax. { ˌpag·yə'rid·ē·ə }

paha [GEOL] A low, elongated, rounded glacial ridge or hill which consists mainly of drift; rock, or windblown sand, silt, or clay but is capped with a thick cover of loess. { pä'hä }

pahoehoe [GEOL] A type of lava flow whose surface is

PAEONIACEAE

The garden peony (*Paeonia lactiflora*), member of the family Paeoniaceae in the order Dilleniales. (*Courtesy of F. E. Westlake, from National Audubon Society*)

brachiopods in the order Terebratulida in which the loop is long and offers substantial support to the side arms of the lophophore. { ˌter·ə·braˌtel·əˈdī·nə }

Terebratulida [INV ZOO] An order of articulate brachiopods that has a punctate shell structure and is characterized by the possession of a loop extending anteriorly from the crural bases, providing some degree of support for the lophophore. { ˌter·ə·braˈtūl·əd·ə }

Terebratulidina [INV ZOO] A suborder of articulate brachiopods in the order Terebratulida distinguished by a short V- or W-shaped loop. { ˌter·ə·brachˌra·laˈdī·nə }

Teredinidae [INV ZOO] The pileworms or shipworms, a family of bivalve mollusks in the subclass Eulamellibranchia distinguished by having the two valves reduced to a pair of small plates at the anterior end of the animal. { ˌter·əˈdinˌəˌdē }

terephthalic acid [ORG CHEM] $C_6H_4(COOH)_2$ A combustible white powder, insoluble in water, soluble in alkalies, sublimes above 300°C; used to make polyester resins for fibers and films and as an analytical reagent and poultry-feed additive. Also known as *para*-phthalic acid; TPA. { ˌterˌəfˌthalˈik ˈasˌəd }

terephthaloyl chloride [ORG CHEM] $C_6H_4(COCl)_2$ Colorless needles with a melting point of 82–84°C; soluble in ether; used in the manufacture of dyes, synthetic fibers, resins, and pharmaceuticals. { ˌterˌəfˈthalˌəˌwil ˈklȯrˌīd }

terete [BOT] Of a stem, cylindrical in section, but tapering at both ends. { təˈrēt }

tergite [INV ZOO] The dorsal plate covering a somite in arthropods and certain other articulate animals. { ˈtərˌjīt }

tergum [INV ZOO] A dorsal plate of the operculum in barnacles. { ˈtərgəm }

terlinguaite [MINERAL] Hg_2OCl A sulfur yellow to greenish-yellow, monoclinic mineral consisting of an oxychloride of mercury. { tərˈlinˌgwəˌīt }

term [SPECT] A set of $(2S + 1)(2L + 1)$ atomic states belonging to a definite configuration and to definite spin and orbital angular momentum quantum numbers S and L. { tərm }

terminal [ARCH] The ornamental finish, decorative element, or termination of an object, item of construction, or structural part. [COMPUT SCI] A site or location at which data can leave or enter a system. [ELEC] **1.** A screw, soldering lug, or other point to which electric connections can be made. Also known as electric terminal. **2.** The equipment at the end of a microwave relay system or other communication channel. **3.** One of the electric input or output points of a circuit or component. { ˈtərmənəl }

terminal air-traffic control [NAV] A separation service offered to aircraft operating in the vicinity of and at airports, involving a system of crewed control towers, radio communications, radar and other position location and guidance facilities, and information processing to make for the safe approach and landing of these aircraft. { ˈtərmənəl ˈerˌtraf·ikˌkənˌtrōl }

terminal area [ELECTR] The enlarged portion of conductor material surrounding a hole for a lead on a printed circuit. Also known as land; pad. { ˈtərmənəl ˈerēə }

terminal bar [CYTOL] One of the structures formed in certain epithelial cells by the combination of local modifications of contiguous surfaces and intervening intercellular substances; they become visible with the light microscope after suitable staining and appear to close the spaces between the epithelial cells of the intestine at their free surfaces. { ˈtərmənəl ˌbär }

terminal block [COMMUN] A cluster of five captive screw terminals at which a telephone pair terminates; the center terminal is for the ground wire, and two other terminals are used for the tip and ring wires. { ˈtərmənəl ˌblȧk }

terminal board [ELEC] An insulating mounting for terminal connections. Also known as terminal strip. { ˈtərmənəl ˌbȯrd }

terminal box [ELEC] An enclosure which includes, mounts, and protects one or more terminals or terminal boards; it may include a cover and such accessories as mounting hardware, brackets, locks, and conduit fittings. { ˈtərmənəl ˌbäks }

terminal bud [BOT] A bud that develops at the apex of a stem. Also known as apical bud. { ˈtərmənəl ˌbəd }

terminal clearance capacity [ENG] The amount of cargo or personnel that can be moved through and out of a terminal on a daily basis. { ˈtərmənəl ˈklirənsˌkəˌpasəd·ē }

terminal control area [NAV] A control area or a portion thereof normally situated at the confluence of air-traffic service routes in the vicinity of one or more major airfields. { ˈtərmənəl kənˈtrōl ˌerēə }

terminal cutout pairs [ELEC] Numbered, designated pairs brought out of a cable at a terminal. { ˈtərmənəl ˈkadˌau̇t ˌperz }

terminal endocarditis *See* verrucous endocarditis. { ˈtərmənəl ˌendōkärˈdīdəs }

terminal equipment [COMMUN] **1.** Assemblage of communications-type equipment required to transmit or receive a signal on a channel or circuit, whether it be for delivery or relay. **2.** In radio relay systems, equipment used at points where intelligence is inserted or derived, as distinct from equipment used to relay a reconstituted signal. **3.** Telephone and teletypewriter switchboards and other centrally located equipment at which wire circuits are terminated. { ˈtərmənəl iˌkwipmənt }

terminal forecast [METEOROL] An aviation weather forecast for one or more specified air terminals. { ˈtərmənəl ˈfȯrˌkast }

terminal guidance [NAV] Guidance of a craft from an arbitrary point, at which midcourse guidance ends, to the destination. { ˈtərmənəl ˈgīdəns }

terminal hair [ANAT] One of three types of hair in man based on hair size, time of appearance, and structural variations; the larger, coarser hair in the adult that replaces the vellus hair. { ˈtərmənəl ˈher }

terminal leg *See* terminal stub. { ˈtərmənəl ˌleg }

terminal moraine [GEOL] An end moraine that extends as an arcuate or crescentic ridge across a glacial valley; marks the farthest advance of a glacier. Also known as marginal moraine. { ˈtərmənəl məˈrān }

terminal nerve [ANAT] Either of a pair of small cranial nerves that run from the nasal area to the forebrain, present in most vertebrates; the function is not known. { ˈtərmənəl ˌnərv }

terminal network [COMPUT SCI] A system that links intelligent terminals through a communications channel. { ˈtərmənəl ˈnetˌwərk }

terminal operations [ENG] The reception, processing, and staging of passengers; the receipt, transit storage, and marshaling of cargo; the loading and unloading of ships or aircraft; and the manifesting and forwarding of cargo and passengers to destination. { ˈtərmənəl ˌäpəˈrāshənz }

terminal pair [ELEC] An associated pair of accessible terminals, such as the input or output terminals of a device or network. { ˈtərmənəl ˈper }

terminal phase [ORD] The period of flight of a missile between the end of midcourse guidance and impact. { ˈtərmənəl ˌfāz }

terminal pressure [ENG] A pressure drop across a unit when the maximum allowable pressure drop is reached, as for a filter press. { ˈtərmənəl ˈpreshər }

terminal radar cab [NAV] An area in the main control tower of an airport where radar control and air-traffic control facilities are located together. { ˈtərmənəl ˈrāˌdärˌkab }

terminal repeater [COMMUN] **1.** Assemblage of equipment designed specifically for use at the end of a communications circuit, as contrasted with the repeater designed for an intermediate point. **2.** Two microwave terminals arranged to provide for the interconnection of separate systems, or separate sections of a system. { ˈtərmənəl riˈpēdər }

terminal room [COMMUN] In telephone practice, a room associated with a central office, private branch exchange, or private exchange, which contains distributing frames, relays, and similar apparatus, except that mounted in the switchboard section. { ˈtərmənəl ˌrüm }

terminal sinus [EMBRYO] The vascular sinus bounding the area vasculosa of the blastoderm of a meroblastic ovum. Also known as marginal sinus. { ˈtərmənəl ˌsīnəs }

terminal speed *See* terminal velocity. { ˈtərmənəl ˌspēd }

terminal station [COMMUN] Receiving equipment and associated multiplex equipment used at the ends of a radio-relay system. { ˈtərmənəl ˌstāshən }

terminal strip *See* terminal board. { ˈtərmənəl ˌstrip }

terminal stub [ELEC] Piece of cable that comes with a cable terminal for splicing into the main cable. Also known as terminal leg. { ˈtərmənəl ˌstəb }

terminal unit [MECH ENG] In an air-conditioning system, a unit at the end of a branch duct through which air is transferred or delivered to the conditioned space. { ˈtərmənəl ˌyünət }

EXHIBIT FF

JONES DAY

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April 27, 2008

BY E-MAIL

John C. Spaccarotella, Esq.
Kirkland & Ellis LLP
153 East 53rd Street
New York, NY 10022-4611

Re: *ON Semiconductor Corp. v. Samsung Electronics Co., Ltd.*
Civil Action No. 1:07-cv-00449 (JJF)
Samsung Electronics Co., Ltd. v. ON Semiconductor Corp.
Civil Action No. 1:06-cv-00720 (JJF)

Dear Mr. Spaccarotella:

Toward clarifying the issues for the Court, please be advised that ON Semiconductor amends its proposed constructions as follows.

'644 Patent:

"programmable termination" – "an electrical circuit that can be configured to provide various levels or degrees for the dissipation or absorption of electrical energy from a transmission line or other device;"

"termination signal" – "a signal that dissipates or absorbs energy from a transmission line or other device;"

"terminate" – "to dissipate or absorb energy from a transmission line or other device;"

'827 Patent:

"altering the flow rate of said solution through said opening" - "to dissipate or absorb energy from a transmission line or other device;"

'177 Patent:

"removing said photoresist pattern" - "getting rid of the photoresist pattern;"

"removing remaining photoresist" - "getting rid of the remaining photoresist;" and

"protective oxide layer" – "an oxide layer of at least 30A thickness that functions to prevent damage to an underlying layer during subsequent processing."

Sincerely,

JONES DAY

Guadalupe M. Garcia

SVI-57355v1

EXHIBIT GG

United States Patent [19]

Vyne

[11] **Patent Number: 4,870,472**

[45] **Date of Patent: Sep. 26, 1989**

[54] **METHOD FOR RESISTOR TRIMMING BY METAL MIGRATION**

[75] Inventor: **Robert L. Vyne, Tempe, Ariz.**

[73] Assignee: **Motorola, Inc., Schaumburg, Ill.**

[21] Appl. No.: **856,257**

[22] Filed: **Apr. 28, 1986**

Related U.S. Application Data

[62] Division of Ser. No. 662,109, Oct. 18, 1984.

[51] Int. Cl.[4] **H01L 27/13**; H01L 29/06; H01L 29/08

[52] U.S. Cl. **357/51**; 357/68; 357/75

[58] Field of Search 357/51, 68, 75

[56] **References Cited**

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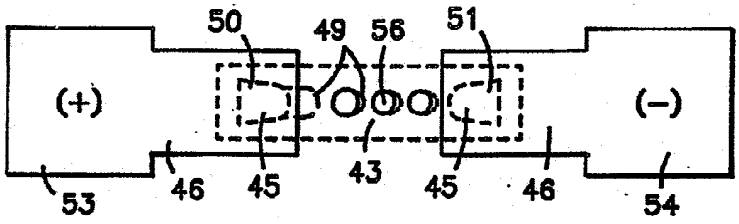
"Detecting Defects in Integrated Semiconductor Circuits"–Hubacher et al., IBM Technical Disclosure Bulletin, vol. 14, No. 9, Feb. 1972, pp. 2615–2617.

Primary Examiner—Rolf Hille
Assistant Examiner—S. V. Clark
Attorney, Agent, or Firm—Mike Bingham

[57] **ABSTRACT**

A method for trimming a diffused or implanted resistor located within an integrated circuit is disclosed. This technique for trimming a resistor requires the use of high current pulses and geometric shaped metal contacts. The current pulses react with the electropositive metal atoms in the thin film conductor and cause the metal atoms to migrate to another location, thus altering the value of the resistor by progressively decreasing the conductivity of the resistor.

5 Claims, 3 Drawing Sheets



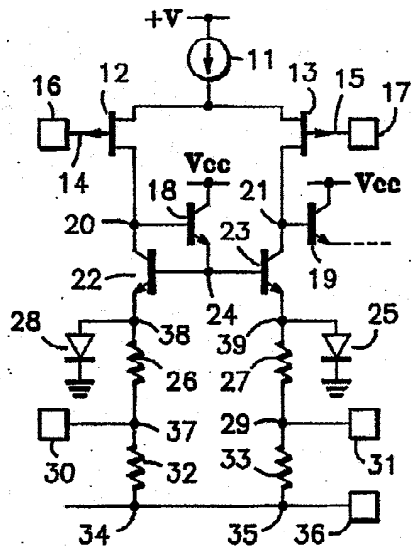


FIG. 1

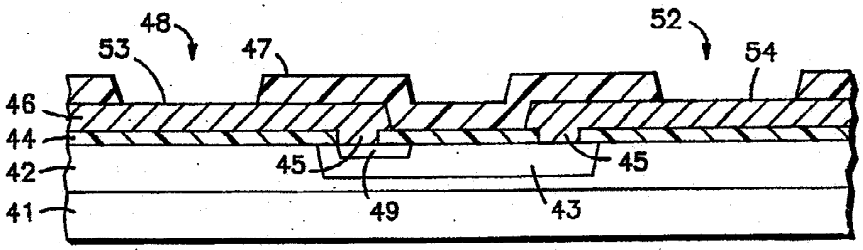


FIG. 2

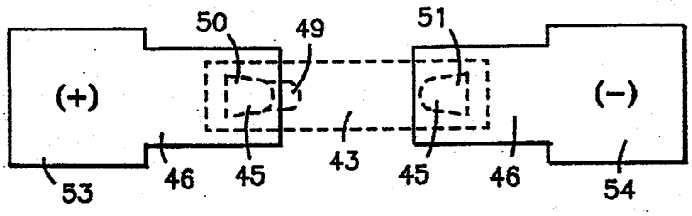


FIG. 3

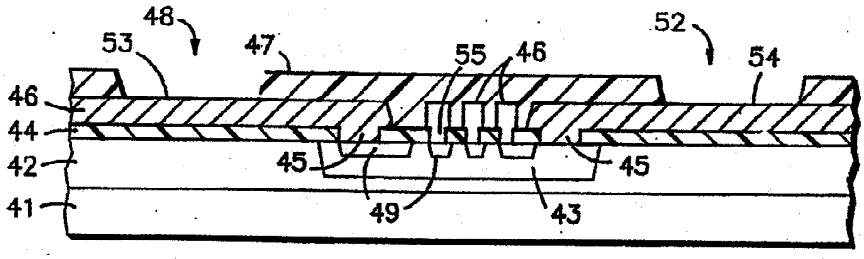


FIG. 4

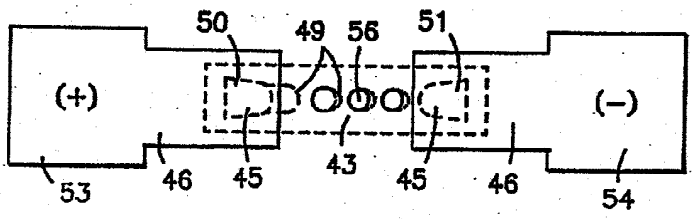


FIG. 5

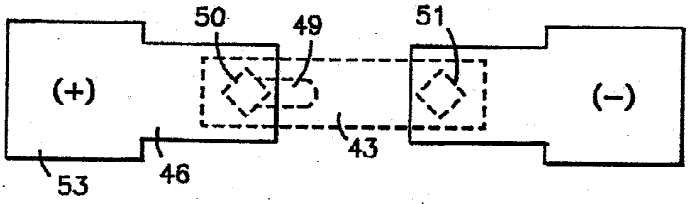


FIG. 6

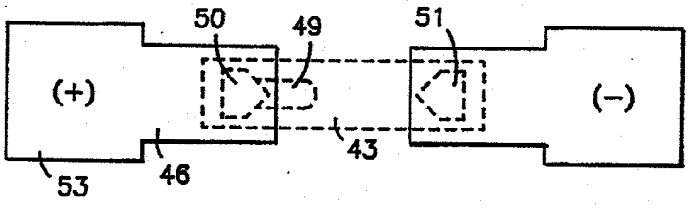


FIG. 7

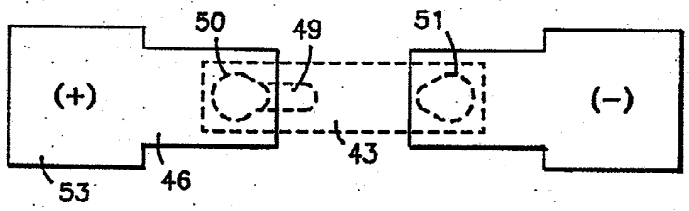


FIG. 8

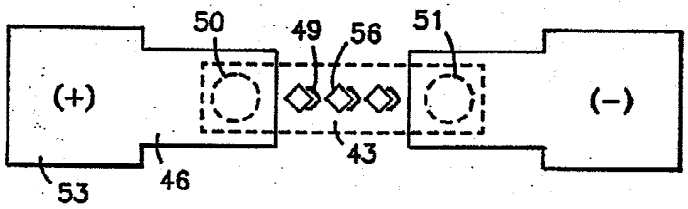


FIG. 9

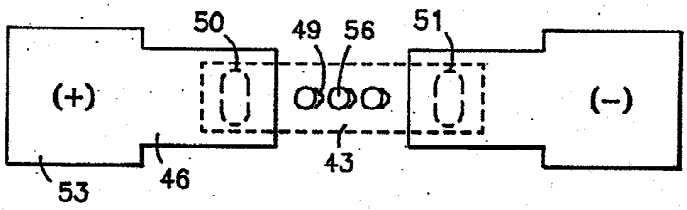


FIG. 10

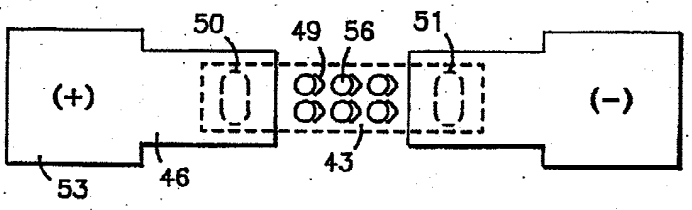


FIG. 11

METHOD FOR RESISTOR TRIMMING BY METAL MIGRATION

This is a division of application Ser. No. 662,109, filed Oct. 18, 1984.

BACKGROUND OF THE INVENTION

This invention relates, in general, to a method for trimming an electrical component that is located within an integrated circuit and, more particularly, to a method for trimming implanted or diffused resistors by the use of metal migration.

The term "trimming" is used to mean the fine adjustment of resistance, capacitance, or inductance in a circuit. As used herein, "metal migration" refers to the movement of metal into a semiconductor crystal (e.g. a resistor). This movement of metal is caused by sending current pulses through the resistor. These pulses are usually of high amplitude and small pulse width.

In the manufacture and packaging of integrated circuits, it is sometimes necessary to "match" (make electrically identical) resistors, transistors, diodes or to set the absolute value of a single electronic device to a certain value, such as trimming a resistor to set a particular current level. For example, trimming of component values on an integrated circuit chip can result in minimizing the input offset voltate of an operational amplifier, or its temperature coefficient of input offset voltage. Trimming of a voltage reference can set the output voltage and temperature coefficient to precise values. Trimming of D/A or A/D converters is commonly done in order to obtain increased accuracy.

Resistor trimming is by far the most common means of adjusting electrical parameters of integrated circuits. Two methods are generally used. The first is to use a trim potentiometer outside the semiconductor device but connected to it through external pins, ie. on a printed circuit board. The second method is to trim a resistor on the integrated circuit die itself.

In the prior art, electronic components, eg. resistors, have been trimmed by mechanical, electrical, or chemical means. For example, mechanical means include abrasion, usually by sandblasting, and laser shaping of a conductive layer. Electrical means include fuse blowing, ie. vaporization of metal by passing high current therethrough and short-circuiting diodes with excessive current. The latter is also known as "zener zapping" since the diodes connected along the resistive elements are zener diodes. Chemically changing the conductivity of the resistor by anodizing the metal is possible but not often used in a production environment.

The known methods of resistor trimming on the die have serious disadvantages. The cost of laser trimming equipment is high. The maintenance and programming of such equipment are extremely critical and costly. Fuse blowing can cause surface contamination and cracks in the protective glass layer which, in turn, cause reliability problems. Zener zapping can require that over twenty per cent of the die be dedicated to resistor trimming.

A further disadvantage in the known methods of resistor trimming on the die is that after the die is trimmed (usually in wafer form) it is scribed and assembled in a package. This assembly process can put stress on the semiconductor chip which can cause the trimmed resistor to change due to piezoresistive effects. It would, therefore, be advantageous to be able to trim an on chip resistor after the integrated circuit die is in the package.

SUMMARY OF THE INVENTION

It is an object of this invention to provide a method for adjusting the value of an electrical component that is located within an integrated circuit by the use of the phenomenon known as metal migration.

Another object of the present invention is to reduce the amount of circuitry that is needed to trim a resistor.

A further object of the present invention is to be able to trim resistors after the die has been sealed in the package.

According to an aspect of the invention there is provided a method for trimming the values of a passive device located within an integrated circuit which includes forming metal contacts at each end of a resistor and causing an electrical current to flow through the resistor in a single direction only. The current causes the metal to migrate from one contact region to the contact region at the opposite end of the resistor. The electrical current is then terminated after a predetermined time.

According to a further aspect of the invention there is provided a semiconductor device including first and second contact regions having mirror apexes.

A more complete understanding of the present invention can be attained by considering the following detailed description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a typical J-FET operational amplifier in which the present invention can be used.

FIG. 2 illustrates a sectional side view of a resistor.

FIG. 3 illustrates the top view of the resistor of FIG. 2

FIG. 4 illustrates a sectional side view of a resistor with additional metal contacts.

FIG. 5 illustrates the top view of the resistor of FIG.4.

FIGS. 6–8 illustrate the top view of a resistor with alternate geometric contacts.

FIGS. 9–11 illustrate the top view of a resistor with additional metal contacts.

DETAILED DESCRIPTION OF THE INVENTION

It is well known in the art that a resistor is constructed on an integrated circuit by implanting or diffusing dopants into a semiconductor material through apertures in a masking material. The contacts are formed by depositing an insulating layer over the resistor region. Openings, called preohmics, are etched into the insulating layer at each end of the resistor. A layer of metal is deposited over the insulating layer and into the preohmics, thus making contacts with the resistor. The shape of the preohmic defines the shape of the metal contact.

Pulsating a direct current through the metal contacts of the diffused resistor results in a metal filament controllably migrating from the positive contact to the negative contact. As the metal migrates through the silicon, the value of the resistor changes. A contact with a sharp corner or a corner with a small radius of curvature will allow the metal to migrate with less current than, for example, a circular contact with a large radius.

The term "contact" refers to the metal region that is touching the resistor region. The geometric metal contacts located on each end of the resistor are also identified as "primary contacts" since they are the ones through which current is supplied. As is more clear from the detailed description herein, additional or secondary contacts are located intermediate the primary contacts. These are not used for supplying current, but merely respond to the current flowing between the primary contacts.

The secondary contacts and the positive primary contact migrate metal at the same time if all the preohmics have the same radius of curvature at the point where the metal begins to migrate. This is important because it defines the geometry of the filament, which is necessary for long term stability of the resistor.

It also has been determined that the geometry of the filament will be determined by the direction of the resistor relative to the crystalographic planes in the wafer substrate, and by the direction of current flow in the resistor.

FIG. 1 illustrates a portion of a typical operational amplifier in which trimmable resistors 32 and 33 are used. Resistors 32 and 33 are trimmed by applying positive pulses to pads 30 or 31. Resistors 26 and 27 along with diodes 28 and 25 protect transistors 22 and 23 from damage during the resistor trim routine. Trimming resistors can also be found in regulators, multipliers, and filters, among other applications. Thus, the circuit of FIG. 1 is representative and not exhaustive of the uses of the present invention.

Current source 11 is connected to the sources of transistors 12 and 13. Bonding pads 16 and 17 are connected to transistors 12 and 13 by way of gate terminals 14 and 15, respectively. The bases of transistors 18 and 19 are connected to nodes 20 and 21 respectively. Nodes 20 and 21 are located between the drains of transistors 12 and 13 and the collectors of transistors 22 and 23 respectively. Node 24 is located between the base of transistor 22 and the base of transistor 23. The emitter of transistor 18 is connected to node 24. The collectors of transistors 18 and 19 are connected to a suitable power supply illustrated as V_{CC}. The emitter of transistor 19 is connected to the next stage in the amplifier, not shown. The emitters of transistors 22 and 23 are connected to nodes 38 and 39, respectively. Diode 28 is connected to node 38 and diode 25 is connected to node 39. Diode 28 and 25 are grounded. Nodes 38 and 39 are connected to resistors 26 and 27, respectively. Resistor 26, pad 30 and resistor 32 are connected to node 37. Resistor 27, pad 31, and resistor 33 are connected to node 29. Resistor 32 and 33 are connected to nodes 34 and 35. respectively. Nodes 34 and 35 are connected to ground pad 36.

The operation of such amplifiers is well known per se in the art and will only be discussed in detail in connection with the trimming of resistors 32 and 33.

FIG. 2 is a sectional view of the various layers that make up a diffused resistor. In this embodiment, substrate 41 comprises a P-type silicon layer covered by an N-type epitaxial layer 42. Resistor 43 comprises an N-type dopant that is diffused into epitaxial layer 42. Insulating layer 44 preferably comprises nitride, although other insulators could be used, and is deposited over the epitaxial layer 42. Openings 45 are etched into nitride layer 44. Metal layer 46 is deposited over the epitaxial layer 42. Openings 45 are etched into nitride layer 44. Metal layer 46 is deposited over the nitridge layer and in openings 45, thus creating metal contacts 50 and 51 (FIG. 3). Protective glass layer 47 is deposited over the metal, and openings 48 and 52 are etched into glass layer 47 to provide access to pads 53 and 54. FIG. 3 does not show the protective glass layer.

When a pulsating current is connected across pads 53 and 54, the metal begins to migrate from metal contact 50, in resistor 43, towards metal contact 51 as represented by region 49. Typical values for current are 250 to 300 milliamps with a range of 250 to 650 milliamps, depending on the resistor characteristics. This current is far in excess of the current flowing through the resistor during normal operation of the amplifier, eg. 100 microamperes. The metal migrates as shown by 49 in the same direction as hole flow and opposite to electron flow. In FIG. 3, pad 53 is connected to a positive voltage source and pad 54 is connected to a negative voltage source or ground. A resistor is trimmed to a given value by adjusting the duration and amount of current passing through it as well as by adjusting the number of current pulses. It is possible to completely short the resistor by pulsing the current for an extended length of time.

While suitable in many applications, the embodiment of FIGS. 2 and 3 is more suited to small changes in resistance. If region 49 is caused to grow significantly, eg. greater than the size of the primary contact as measured in the same direction, then some drift may be encountered in operation of the device. To correct for the drifting value, a further embodiment of this invention is shown in FIGS. 4 and 5.

In this embodiment, a plurality of secondary contacts are added so that the migration is spread over several regions located more or less along a straight line between the primary contacts. Substrate 41 is covered by epitaxial layer 42. Resistor 43 is diffused into epitaxial layer 42. Insulating layer 44 preferably comprises nitride, is located on top of the epitaxial layer. Openings 45 and 55 are etched into nitride layer 44. Openings 55 may have any shape and are merely illustrated as circular in shape. Metal 46 is deposited over the nitride and into 45 and 55, thus creating metal contacts 50, 51, and 56. Contacts are known as secondary contacts. Protective glass layer 47 is deposited over the metal, and openings 48 and 52 are etched into the glass to provide access to pads 53 and 54. FIG. 5 does not show the protective glass layer. Applying a pulsating current having a positive polarity at pad 53 and a negative polarity at pad 54 the metal begins to migrate from metal contact 50, toward metal contact 51 as illustrated by regions 49. Each of the circular metal contacts 56 has metal migrating toward contact 51. During trim, these secondary contacts produce shorter average filament lengths, which has been found to stabilize the trimmed resistor value during high temperature life tests.

FIGS. 6–8 illustrate alternative embodiments of shapes for primary contacts 50 and 51. Secondary contacts may be added or not, as desired. The primary contacts are also characterized by mirrored apexes pointing at each other and having a radius of curvature which is small relative to the size of the contact.

In an alternative embodiment of the present invention illustrated in FIGS. 9–11, there is no migration from the primary contacts. In addition, secondary contacts are located between the primary contacts and are of a design to allow the metal to migrate. This embodiment prevents the occurrence of an open circuit at the primary contact region.

A number of variations in the basic process are possible. Substrate 41 can be N-type and epitaxial layer 42 a

P-type layer. Resistor 43 can be implanted and/or be P-type. Insulating layer 44 can comprise oxide or a combination of oxide and nitride or polyimide. Metal layer 46 can comprise pure aluminum, aluminum alloy such as aluminum copper, aluminum silicon, or aluminum copper silicon or other metal. The protective layer can comprise doped silicon dioxide, silicon nitride, plasma silicon, polyimide, or the like.

The advantages of resistor trimming by metal migration (RTMM) are numerous. Conventional processes and test equipment can be used to manufacture and trim the diffused RTMM resistor, unlike expensive thin film processes with laser trim. The migrating metal occurs in the silicon body of the RTMM resistor, which does not damage the protective passivation on the surface of the I.C. chip. This is not the case with laser trim or fuse blowing techniques. For laser trimming, elaborate test programs must be written to increment the laser to the proper targets. RTMM does not require this. Trimming by zener zapping requires complicated circuitry along with high voltage protection schemes. Also, it consumes typically twenty per cent of the total die area. Trimming with RTMM requires very little die area. Trimming with the RTMM resistor can be done after the I.C. chip is sealed in the package, which will trim out any inaccuracies caused by package stresses. Since RTMM is an analog trimming method, much more accuracy can be achieved with computer control than can be achieved by zener zapping on the die.

There is thus provided by the present invention as an improved method for trimming resistors. It requires no special processing and produces more accurate resistors.

Having thus described the invention, it will be apparent to those skilled in the art that various modifications can be made within the spirit and scope of the present invention. For example, while the pre-ohmic holes are illustrated as uniformly spaced in FIGS. 4, 5, and 9–11, they need not be. Also, as previously discussed, the present invention can be implemented in a variety of semiconductor materials and conductivity types.

What is claimed is:

1. A resistor formed in a semiconductive substrate, comprising:

a resistive region in said substrate having first and second ends;

a first contact for contacting said region proximate said first end;

a second contact for contacting said region proximate said second end; and

a metal filament formed in said region and extending from said first contact toward said second contact.

2. A resistor device formed in a substrate, comprising:

a semiconductor region formed in said substrate and having first and second ends;

a first metallic contact for contacting said region proximate said first end;

a second metallic contact for contacting said region proximate said second end, said first metallic contact having an apex directed toward said second metallic contact;

at least one additional metallic contact for contacting said region intermediate said first and second metallic contacts and having an apex directed toward said second metallic contact; and

a first metal filament formed in said region and extending from said first metallic contact toward said second metallic contact.

3. A device according to claim 2 further comprising a second metal filament formed in said region and extending from said at least one additional contact toward said second contact.

4. A resistor manufactured by:

providing a resistive semiconductive region;

providing first and second metal contacts for contacting said region; and

passing at least one current pulse from said first contact to said second contact whereby metal migrates from said first contact toward said second contact to reduce the resistance therebetween.

5. A passive semiconductor device formed in a substrate comprising:

a semiconductive region formed in said substrate having first and second ends;

a first contact for contacting said region proximate said first end;

a second contact for contacting said region proximate said second end;

at least one additional contact for contacting said region intermediate said first and second contacts; and

a metal filament formed in said region and extending from said additional contact toward said second contact.

* * * * *

EXHIBIT HH

McGRAW-HILL ELECTRONICS DICTIONARY

FIFTH EDITION

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dummy load A dissipative device used at the end of a transmission line or waveguide to convert transmitted energy into heat, so essentially no energy is radiated outward or reflected back to its source.

dump 1. To withdraw all power from a computer accidentally or intentionally. 2. In digital computer programming, to transfer all or part of the contents of one section of computer memory into another section.

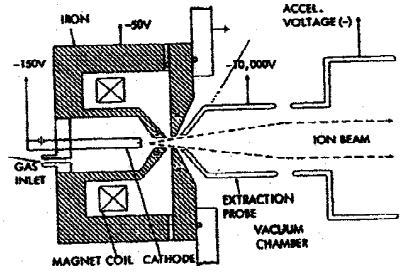
dump check A computer check that usually consists of adding all the digits during dumping and verifying the sum when retransferring.

dunking sonar *Dipping sonar.*

duobinary frequency modulation Frequency modulation using three signaling frequencies instead of two for transmitting digital data. The center frequency represents binary 0, and the two outside frequencies represent 1. The code has some error-detecting capability because the 1 frequency always relates back to the frequency of the previous 1. Used in some modems for data transmission over wire lines.

duodecimal number system A number system using the equivalent of the decimal number 12 as a base.

duoplasmatron An ion-beam source in which electrons from a hot filament are accelerated sufficiently to ionize a gas by impact. The resulting positive ions are drawn out by high-voltage electrons and focused into a beam by electrostatic lens action. Used in mass spectrometers.



Duoplasmatron ion-beam source.

duplex *Duplex operation.*

duplex channel A communication channel providing simultaneous transmission in both directions.

duplexer A switching device for radar that permits alternate use of the same antenna for both transmitting and receiving. It contains the TR switch that blocks out the receiver when the transmitter is operating. Other forms of duplexers serve for two-way radio communication with a single antenna at lower frequencies.

duplexing *Duplex operation.*

duplex operation The operation of associated transmitting and receiving apparatus concurrently, as in ordinary telephones, without manual switching between talking and listening periods. A separate frequency band is required for each direction of transmission. Also called duplex and duplexing.

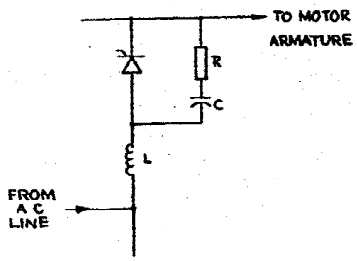
duplication check A computer check that requires the results of two independent performances (either concurrently on duplicate equipment or at a later time on the same equipment) in the same operation to be identical.

DUT Abbreviation for *device under test.*

duty cycle 1. The ratio of working time to total time for an intermittently operating device. Usually expressed as a percentage. 2. The ratio of pulse width to the interval between like portions of successive pulses. Usually expressed as a percentage.

DUV Abbreviation for *deep ultraviolet* and *data under voice.*

dv/dt protection Protection of a circuit or device from excessive voltage rate-of-change, usually achieved with a resistor-coil-capacitor network.



Dv/dt protection for thyristor in motor control circuit, using RLC network around thyristor.

DVM Abbreviation for *digital voltmeter.*

DVOM Abbreviation for *digital volt-ohm-milliammeter.*

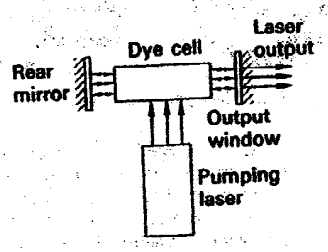
dwell A controlled time interval or delay during which a specified action occurs, such as the closing of contacts or the maximum lift position of a cam.

dwell meter An instrument for measuring the time that distributor breaker points are closed in an automobile ignition system. The reading is usually given in angular degrees through which the distributor cam rotates from the instant the contact points close until they open again.

DX Abbreviation for distance reception, related to the reception of, or communication with, distant radio stations.

dyadic operation Simultaneous operation on two operands in a computer.

dye laser A liquid laser in which the lasing material is an active organic fluorescent material dissolved in a solvent. One organic dye used for this purpose is anthracene. The dye can be excited by another laser, a flashlamp, or some other pulsed light source, to give either pulsed or continuous tunable output in the visible spectrum. Tuning is achieved by such means as rotating a diffraction grating or



Dye laser using separate laser for pumping.